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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,372	12/29/2000	Anthony X. Jarvis	00-BN-051 (STMI01-00051)	8275

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EXAMINER	
O'BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

P2C9

Office Action Summary	Application No.	Applicant(s)	
	09/751,372	JARVIS ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 and 16 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration Fee as received on 4/16/2001 and Drawings as received on 4/16/2001.

Drawings

3. The drawings are objected to because of the following minor informalities:

   a. Figure 6 cites reference number "535" as being both a "Latch" and a "Shifter." Please correct this to refer to the "Latch" using reference number "525", and the "Shifter" as reference number "535."

4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Objections

7. Claims 1, 4, 6, 10, 14, 17 and 19 are objected to because of the following informalities:

   a. Regarding claim 1, the language in the second to last paragraph states "one of a) shifting, b) sign extending, and c) zero extending," language which is in the alternative format. Please replace the "and" in the above statement with "or" in order to correctly use the alternative format. Also see claims 4, 6, 14, 17 and 19 for similar corrections.

   b. Regarding claim 10, the preamble recites the language "for use in a processor comprising an N-Stage execution pipeline, a data cache, and a plurality of registers" in the beginning of the first sentence. Please reword the claim language

to more distinctly point out and clearly word what it is that the claimed method does. For example, a new preamble may be "A method for loading a first data value from a data cache into a target register of a plurality of registers comprised in an N-Stage execution pipeline, the method comprising the steps of."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenley, U.S. Patent No. 5,761,469, in view of Dye, U.S. Patent No. 6,412,061.

10. Regarding claims 1 and 14, taking claim 14 as exemplary, Greenley has taught a processing system comprising:

a. A data processor (100 of Fig.1).

b. A memory coupled to said data processor (see Col.1 lines 41-43).

c. Wherein said data processor comprises:

i. An instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline (see Col.1 lines 34-40).

ii. A data cache (180 of Fig.1) capable of storing data values used by said pending instruction (see Col.1 lines 42-43).

iii. A plurality of registers (150 of Fig.1) capable of receiving said data values from said data cache (see Col.1 lines 41-45).

iv. A load store unit (130 of Fig.1) capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation (see Col.1 lines 15-21, 63-67 and Col.2 lines 1-7, 13-15).

v. A shifter circuit (160,170 of Fig.1) associated with said load store unit capable of one of a) shifting (see Col.2 lines 19-31), b) sign extending (see Col.2 lines 48-54), and c) zero extending (see Col.2 lines 45-47) said first data value prior to loading said first data value into said target register.

11. Greenley has not explicitly taught bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

12. However, Dye has taught the bypassing of portions of a circuit that are not needed in order to reduce the latency inherent with such circuitry as instructions are executed (see Abstract and Col.3 lines 2-11, 35-43). Greenley has taught a sign extension unit (160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (see Col.2 lines 48-50). This implies that when fetched data occupies the entire register no sign extension is necessary because there are no unoccupied bits, thereby making the sign extension and alignment units unnecessary in certain circumstances. Therefore, one of ordinary skill in the

art would have found it obvious to modify Greenley to include a bypass path around the unused sign extension and aligning units because doing so would reduce the latency required to load data (see Dye Col.3 lines 2-11 and 35-43).

13. Greenley has also not explicitly taught the processing system comprising a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

14. However, Dye has taught the inclusion of a graphics coprocessor and a memory mapped frame buffer connected to the processor via system bus which perform specific tasks in order to free up the main processor to perform other general operations (see Col.2 lines 21-35). Therefore, one of ordinary skill in the art would have found it obvious to include a graphics coprocessor and frame buffer as a memory-mapped peripheral circuit in the processor of Greenley in order to allow the main processor to perform general tasks in order to free up processor cycles (see Dye, Col.2 lines 21-25).

15. Claim 1 is nearly identical to claim 14. Claim 1 differs in its lack of a main memory and memory-mapped peripheral circuits, but comprises the same data processor as claim 14, and is therefore rejected for the same reasons.

16. Regarding claims 2 and 15, taking claim 15 as exemplary, Greenley in view of Dye has taught the processing system as set forth in claim 1, wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation (see above rejection of claim 1, as well as Dye Col.3 lines 2-11 and 35-43). While Greenley has taught a different register size than the applicant (see Col.2 lines 17-19), the situation when a register has no unoccupied bits after being loaded with data from a data cache remains the same,

with the size of the register and word being moot. Therefore Greenley's loading of a double word has the same consequences as the applicant's loading of a word.

17. Claim 2 is nearly identical to claim 15. Claim 2 differs in its parent claim, but comprises the same data processor as claim 15, and is therefore rejected for the same reasons.

18. Regarding claims 3 and 16, taking claim 16 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 2, wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles (see Col.4 lines 17-20). However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

19. Claim 3 is nearly identical to claim 16. Claim 3 differs in its parent claim, but comprises the same data processor as claim 16, and is therefore rejected for the same reasons.

20. Regarding claims 4 and 17, taking claim 17 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 1, wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation (see Greenley Col.2 lines 17-20, 24-30, 46-47).

21. Claim 4 is nearly identical to claim 17. Claim 4 differs in its parent claim, but comprises the same data processor as claim 17, and is therefore rejected for the same reasons.

22. Regarding claims 5 and 18, taking claim 18 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 4, wherein said shifter circuit loads said shifted first data value into said target register at the end of two machine cycles (see Col.4 lines 17-20), but has not explicitly taught the load taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

23. Claim 5 is nearly identical to claim 18. Claim 5 differs in its parent claim, but comprises the same data processor as claim 18, and is therefore rejected for the same reasons.

24. Regarding claims 6 and 19, taking claim 19 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 1, wherein said shifter circuit one of a) shifts, b) sign extends, and c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation (see Greenley Col.2 lines 17-20, 36-40, 46-47).

25. Claim 6 is nearly identical to claim 19. Claim 6 differs in its parent claim, but comprises the same data processor as claim 19, and is therefore rejected for the same reasons.

26. Regarding claims 7 and 20, taking claim 20 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 6, wherein said shifter circuit loads said shifted first data value into said target register at the end of two machine cycles (see Col.4 lines 17-20), but has not explicitly taught the load taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as byte load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenley in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus

taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

27. Claim 7 is nearly identical to claim 20. Claim 7 differs in its parent claim, but comprises the same data processor as claim 20, and is therefore rejected for the same reasons.

28. Regarding claims 8 and 21, taking claim 21 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 1, but has not explicitly taught wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

29. However, Dye has taught the multiplexer (322 of Fig.3) selecting between data from the current stage and data that has been bypassed from the prior stage (see Fig.3 and Col.9 lines 41-55). As taught above in the rejection of claim 1, Greenley in view of Dye has taught the use of a bypass circuit around the sign extension and alignment units when certain types of load instructions are executed. Because not all load instructions are to use the bypass, such as load byte and load half-word instructions, the circuit must have the ability to select between using the bypass circuit or not. Therefore, one of ordinary skill in the art would have found it obvious to use the multiplexer (Dye, 322 of Fig.3) to select between data coming from the data cache and the sign extension/alignment units so that the latter units are not always bypassed so the correct datapath is chosen.

30. Claim 8 is nearly identical to claim 21. Claim 8 differs in its parent claim, but comprises the same data processor as claim 21, and is therefore rejected for the same reasons.

31. Regarding claims 9 and 22, taking claim 22 as exemplary, Greenley in view of Dye has taught the data processor as set forth in claim 8, wherein said multiplexer (Dye, 322 of Fig.3) has

a second input channel coupled to an output of said shifter circuit. As taught above in the rejection of claim 8, the multiplexer (Dye, 322 of Fig.3) selects between the output of the data cache and the sign extension/alignment units so that the correct datapath is chosen.

32. Claim 9 is nearly identical to claim 22. Claim 9 differs in its parent claim, but comprises the same data processor as claim 22, and is therefore rejected for the same reasons.

33. Regarding claim 10, Greenley has taught for use in a processor comprising an N-stage execution pipeline (see Col.1 lines 34-40), a data cache (180 of Fig.1), and a plurality of registers (150 of Fig.1), a method of loading a first data value from the data cache into a target one of the registers, the method comprising the steps of:

a. Determining if a pending instruction in the execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation (see Col.1 lines 63-67, Col.2 lines 1-7, 17-19 and Col.5 lines 13-24).

b. In response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register (see Col.2 lines 24-31).

c. In response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register (see Col.2 lines 35-40).

34. Greenley has not explicitly taught where in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit.

35. However, Dye has taught the bypassing of portions of a circuit that are not needed in order to reduce the latency inherent with such circuitry as instructions are executed (see Abstract and Col.3 lines 2-11, 35-43). Greenley has taught a sign extension unit (160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (see Col.2 lines 48-50). This implies that when fetched data occupies the entire register no sign extension is necessary because there are no unoccupied bits, thereby making the sign extension and alignment units unnecessary in certain circumstances. Therefore, one of ordinary skill in the art would have found it obvious to modify Greenley to include a bypass path around the unused sign extension and aligning units because doing so would reduce the latency required to load data (see Dye Col.3 lines 2-11 and 35-43).

36. Regarding claim 11, Greenley in view of Dye has taught the method as set forth in claim 10, wherein the step of transferring the first data value requires two machine cycles during a load word operation (see Col.4 lines 17-20). However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension. While Greenley has taught a

different register size than the applicant (see Col.2 lines 17-19), the situation when a register has no unoccupied bits after being loaded with data from a data cache remains the same, with the size of the register and word being moot. Therefore Greenley's loading of a double word has the same consequences as the applicant's loading of a word. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenley in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

37. Regarding claim 12, Greenley in view of Dye has taught the method as set forth in claim 10, wherein the step of transferring the first data value requires two machine cycles during a load half-word operation (see Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be

equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

38. Regarding claim 13, Greenley in view of Dye has taught the method as set forth in claim 10 wherein the step of transferring the first data value requires two machine cycles during a load byte operation (see Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as during the applicant's load word or Greenley's load double word, the data processor as configured above will execute the load instruction one cycle faster (see Dye Col.3 lines 2-11, 35-43). This will create a latency of one cycle for those load instructions which bypass the sign extension unit, and two cycles for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Dye have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Dye (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the

references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

40. Tamura et al, U.S. Patent No. 6,311,199, has taught a method of sign extending and aligning data from a data cache that includes a mode where data the same width of a register is not sign extended.

41. Thatcher et al, U.S. Patent No. 6085,289, has taught a method for loading data from a data cache which formats and sign extends the data to a correct format.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
11/14/2003

EDDIE CHAN
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